assembler/disassembler 38 and the buffer DPR 42 pass through Error Detection And Correction circuitry (EDAC) 44.

An arrangement of state machines, three in this illustrative embodiment comprising a Lower Machine 46, a Middle Machine 48 and an Upper Machine 50, facilitate movement of user data between the buffer DPR 42 and the backplane 170 to Global Memory (GM).

The Lower Machine ("LM") 46 controls "lower side" data transfers, including the handshake protocol between the assembler/disassembler 38, the EDAC 44 and the buffer DPR 42, for transferring data on GM reads and writes. For example, when an assembler/disassembler 38 needs to transfer data to GM (i.e. a write operation), it sends out a request, which is subject to arbitration as described in detail hereinafter. The LM 46 receives information regarding a pipeline data transfer and sends an acknowledge back to the assembler/disassembler which won the arbitration. The assembler/disassembler that owns the right to transfer begins a data transfer over the SDIO bus 40, through the EDAC 44 to the buffer DPR 42. Similarly, on read operations the LM 46 controls transfers from the buffer DPR 42 through the EDAC 44 over the SDIO bus 40 to the assembler/disassembler(s) 38.

The Middle Machine 48 ("MM") effectively oversees control of all data movement to and from the GM. Although not directly in the data path, it is responsible for coordinating control between

the various elements that comprise the data transfer channels. The MM 48 is interconnected to the LM 46 and the Upper Machine 50, and various global memory data path elements. The MM 48 provides control and coordination between the upper and lower sides of the buffer DPR 42. The lower (or Lower Machine) side of the MM 48 connects to the assembler/disassembler 38 of each pipe and the LM 46. The upper (or Upper Machine) side of the MM 48 connects to the backplane 170 and the Upper Machine, which in turn connects to GM. The actual data transfers between the buffer DPR and GN are controlled by the Upper Machine and Lower Machine.

The Upper Machine 50 ("UM") implements the backplane protocol to accomplish data transfers between the GM connected to the backplane 170 and the ESCON interface according to the invention. The MM 48 determines a pipe that needs servicing. The UM 50 receives, from the MM 48, information regarding the pipe to be serviced and requests backplane access. The MM 48 provides the address and the UM 50 provides the command and transfer length to the backplane 170 over a plurality of transceivers 52, 54, 56. When the data transfer phase begins, the UM 50 manages the buffer DPR 42 address and control signals, and provides a clock on write operations. Data is transferred from the buffer DPR 42 to the backplane 170 over a backplane transceiver 58.

beginning of time when the ESCON interface is first powered on. The service processor 70 prepares the board, loads all the FPGAs, brings up the board, runs diagnostics, and then once it has determined that everything is functional it will turn on the line processors. The service processor is a high end, low power, high performance and low cost processor with the ability to be interfaced into a system, such as a power PC 603E or the like.

The service processor 70 also performs system wide services. When there is a system wide interrupt it is delivered to the service processor 70, which acts upon the interrupt. The service processor 70 determines whether it is appropriate to interrupt the data transfer that is in progress or not.

The service processor 70 has a Small Computer System Interface (SCSI) port. In the case of a power failure the service processor 70 shuts down the ESCON line(s) and then dumps the data to disk.

The service processor 70 is further responsible for consolidating some of the operations from each of the line interfaces/processors 60. If all of the line processors performed all of the accesses to the backplane 170 themselves there would be numerous accesses. The line processors defer and consolidate their actions onto the service processor 70 so that the service processor can do the operation on behalf of the whole